| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/812,056 | 03/30/2004 | Masahiro Ito | Q80548 | 1303 |

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|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2629 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 12/10/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on <u>18 September 2008</u>.

2a) ☒ This action is **FINAL**.          2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) <u>1-19</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) <u>9</u> is/are allowed.

6) ☒ Claim(s) <u>1-5,7,8 and 10-19</u> is/are rejected.

7) ☐ Claim(s) <u>6</u> is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>30 March 2004</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☒ All    b) ☐ Some * c) ☐ None of:

        1. ☒ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____.

        3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

# DETAILED ACTION

## *Claim Objections*

1.      Claim 13 is objected to because of the following informalities: RGB. Appropriate

correction is required. Examiner suggests using "Red, Green and Blue (RGB)" The first

time "RGB" is introduced and then "RGB" can be used the rest of the time for each of

the independent claims.


2.      Claim 17 is objected to because of the following informalities:  the claim should

be labeled "(new)".  Appropriate correction is required. Examiner suggests inserting in

parenthesis the status of the claim.


## *Claim Rejections - 35 USC § 103*

3.      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

4.      The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

    1.      Determining the scope and contents of the prior art.
    2.      Ascertaining the differences between the prior art and the claims at issue.
    3.      Resolving the level of ordinary skill in the pertinent art.
    4.      Considering objective evidence present in the application indicating
            obviousness or nonobviousness.

5.      Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Atsushi (JP Publication number 2002-221950) hereinafter Atsushi in view of

Kitagawa et al (2002/0063784) hereinafter, Kitagawa.

6.      In regards to claim 1, Atsushi teaches a video processor comprsing: a bit rate

converter for converting (fig. 1 (10)) an M-bit input (fig.  Input into 10) video signal to an

N-bit (fig. 1 output of 10) output video signal by retaining grayscale levels (0068-0071),

wherein N is smaller than M (0071); and

        a  pseudo-tone processing means (fig. 1 (11)) and frame memory  (fig. 1 (10)),

when said N-bit output (0086) video signal of said bit rate converter (fig. 1 (10))

corresponds to one of the plurality of N-bit input grayscale levels (0071-0082)

        said pseudo-tone processing means (fig. 1 (11)) and frame memory  (fig. 1 (10))

delivering one of a plurality of K-bit output grayscale levels to said display device (fig. 1

(13 to 14)).

        Atsushi fails to teach a gamma correction memory in which a plurality of N-bit

input grayscale levels are mapped to a plurality of K-bit output grayscale levels which

are distributed on a non-linear curve corresponding to a non-linear curve on which

grayscale levels of a display device are distributed.

        However, Kitagawa teaches a gamma correction memory (fig. 1 (13) [0030]) in

which a plurality of N-bit input grayscale levels (fig. 1 (11 bits of 13) [0020]) are mapped

(fig. 7 [0029]) to a plurality of K-bit output grayscale levels which are distributed ([0020)

on a non-linear curve (fig. 7) corresponding to a non-linear curve on which grayscale

levels ([0020 and 0029]) of a display device are distributed [0020].

It would have been obvious to one of ordinary skill in the art, at the time of the

invention, to modify Atsushi to **substitute** the use of a gamma correction memory, for

the memory (fig. 1 (10)) of Atsushi, as taught by Kitagawa in order to perform gamma

correction in order to properly show shadow detail in RBG images and to avoid

gradation deterioration in gray zones ([0005] of Kitagawa).


7.      In regards to claim 17, Atsushi teaches a video processor comprising (abstract

fig. 1):

a first component processor for processing a first component of an RGB color

model (fig. 1 (10) R);

a second component processor for processing a second component of the RGB

color model (fig. 1 (10) G); and

a third component processor for processing a third component of the RGB color

model (fig. 1 (10) B), Examiner notes first that Applicant has not claimed wherein the

component processors are separate and distinct and second from 0071 the component

processing is carried out separately inside fig. 1 (10).

wherein each of the first, second and third components processor comprises:

a bit rate converter for converting (fig. 1 (10)) an M-bit input (fig. Input into 10)

video signal to an N-bit (fig. 1 output of 10) output video signal by retaining grayscale

levels (0068-0071), wherein N is smaller than M (0071); and

a pseudo-tone processing means (fig. 1 (11)) and frame memory (fig. 1 (10)),

when said N-bit output (0086) video signal of said bit rate converter (fig. 1 (10))

corresponds to one of the plurality of N-bit input grayscale levels (0071-0082)

said pseudo-tone processing means (fig. 1 (11)) and frame memory (fig. 1 (10))

delivering one of a plurality of K-bit output grayscale levels to said display device (fig. 1

(13 to 14)).

Atsushi fails to teach a gamma correction memory in which a plurality of N-bit

input grayscale levels are mapped to a plurality of K-bit output grayscale levels which

are distributed on a non-linear curve corresponding to a non-linear curve on which

grayscale levels of a display device are distributed.

However, Kitagawa teaches a gamma correction memory (fig. 1 (13) [0030]) in

which a plurality of N-bit input grayscale levels (fig. 1 (11 bits of 13) [0020]) are mapped

(fig. 7 [0029]) to a plurality of K-bit output grayscale levels which are distributed ([0020]

on a non-linear curve (fig. 7) corresponding to a non-linear curve on which grayscale

levels ([0020 and 0029]) of a display device are distributed [0020].

It would have been obvious to one of ordinary skill in the art, at the time of the

invention, to modify Atsushi to **substitute** the use of a gamma correction memory, for

the memory (fig. 1 (10)) of Atsushi, as taught by Kitagawa in order to perform gamma

correction in order to properly show shadow detail in RBG images and to avoid

gradation deterioration in gray zones ([0005] of Kitagawa.

8.      In regards to claim 3, Atsushi as modified by Kitagawa teaches wherein said K-

bit (fig.1 (output to display of Atsushi) output grayscale ([0029] of Kitagawa) levels

value, are interpolated grayscale ([0029] of Kitagawa) levels of the N-bit input (fig. 1

(reduced bits from 10) of Atsushi) grayscale levels ([0029] of Kitagawa). Examiner notes

the interpolation is part of the non-linear gamma correction as taught by Kitagawa and

the N-bits and K-bits are taught by Atsushi, since the gamma correction memory of

Kitagawa was substituted.

9.      In regards to claim 10, Atsushi discloses wherein M is 18 bits (fig. 1 RGB 6:6:6)

[0006-0007, 0077]).

        Atsushi does not disclose expressly wherein M is 10.

        At the time the invention was made, it would have been an obvious matter of

design choice to a person of ordinary skill in the art to make M equal to 10 bits because

Applicant has not disclosed that wherein M is 10 provides an advantage, is used for a

particular purpose, or solves a stated problem. One of ordinary skill in the art,

furthermore, would have expected Applicant's invention to perform equally well with 18,

16, 12  or any other bit value depending on the input signal because the device may be

given different input signals.

Therefore, it would have been obvious matter of design choice to modify Atsushi to obtain the invention as specified in claims [s].

10.     In regards to claim 11, Atsushi discloses wherein N is 12 bits (fig. 1 RGB 6:6:6) [0006-0007, 0077]).

Atsushi does not disclose expressly wherein N is 8.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to make N equal to 8 bits because Applicant has not disclosed that wherein N is 8 provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with 18, 16, 12  or any other bit value because using various values will determine the amount of memory saved.

Therefore, it would have been obvious matter of design choice to modify Atsushi to obtain the invention as specified in claims [s].

11.     In regards to claim 12, Atsushi discloses wherein K is 18 bits (fig. 1 RGB 6:6:6) [0006-0007, 0077]).

Atsushi does not disclose expressly wherein K is 8.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to make K equal to 8 bits because Applicant has not disclosed that wherein K is 8 provides an advantage, is used for a

particular purpose, or solves a stated problem. One of ordinary skill in the art,

furthermore, would have expected Applicant's invention to perform equally well with 18,

16, 12 or any other bit value because a table stores trans values and as Atsushi states

"many bits can also be formed to other bit values" [0077] .

Therefore, it would have been obvious matter of design choice to modify Atsushi

to obtain the invention as specified in claims [s]. Examiner also notes that claim 12

depends from claim 1 and do not require that M be 10 or N is 8 since claims 10 and 11

are separate dependent claims.


12.     In regards to claim 13 Atsushi teaches the video processor of claim 1, wherein

the M-bit input video signal corresponds to a first component of an RGB color model

(abstract and fig 1 RGB input to 10).


13.     In regards to claim 14, Atsushi teaches the video processor of claim 13, wherein

the first component is a red component (fig. 1 R of RGB).


14.     In regards to claim 15, Atsushi teaches the video processor of claim 13, wherein

the bit rate converter converts the M-bit input video signal corresponding to the first

component independent of signals corresponding to a second and a third component of

the RGB color model (fig. 1 (RGB) [0071]).

15.     In regards to claim 16. Atsushi teaches the video processor of claim 13, wherein

the N-bit input grayscale levels correspond to the first component of an RGB color

model [0074-0077]. Examiner notes that the N-bit input grayscales correspond to the

first component R.


16.     In regards to claim 18, Atsushi discloses wherein N is 12 bits (fig. 1 RGB 6:6:6)

[0006-0007, 0077]).

        Atsushi does not disclose expressly wherein N is 6.

        At the time the invention was made, it would have been an obvious matter of

design choice to a person of ordinary skill in the art to make N equal to 6 bits because

Applicant has not disclosed that wherein N is 8 provides an advantage, is used for a

particular purpose, or solves a stated problem. One of ordinary skill in the art,

furthermore, would have expected Applicant's invention to perform equally well with 18,

16, 12  or any other bit value because a table stores trans values and as Atsushi states

"many bits can also be formed to other bit values" [0077] .

        Therefore, it would have been obvious matter of design choice to modify Atsushi

to obtain the invention as specified in claims [s].


17.     In regards to claim 19, (new), Atsushi teaches the video processor of claim 1,

wherein N is less than K.(fig. N is equal to 12 bits and the output of 12 is 18 bits).

18.     In regards to claim 4, Atsushi teaches wherein K is equal to M (0082) and (fig. 1 (12)).

19.     Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi and Kitagawa further in view of Lumelsky et al (5,196,924) hereinafter, Lumelsky,

20.     In regards to claim 2, Atsushi and Kitagawa discloses the limitations of claim 1,

Atsushi and Kitagawa differ from the claimed invention in that Atsushi does not disclose wherein K is equal to N.

However, Lumelsky discloses K is equal to N. (col. 5, lines 25-25)

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi and Kitagawa to include the use of K is equal to N as taught by Lumelsky in order to further conserve memory.

21.     Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi in view of Kitagawa further in view of Pether et. al (US 6,801,925) hereinafter, Pether.

22.     In regards to claim 5, Atsushi and Kitagawa differ from the claimed invention in that Atsushi and Kitagawa do not disclose wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal, representing the truncated lower significant bits by a different number of binary-1 's, and distributing the binary- 1's over a varying number of subsequent frames depending on the truncated lower significant bits.

However, Pether teaches a system and method for wherein said bit rate

converter (fig. 5 (100)) comprises means for truncating lower significant bits (fig. 5 of

the M-bit video signal (col. 3, lines 49-50), representing the truncated lower significant

bits (fig. 5 "LSBs") by a different number of binary-1 's, and distributing the binary- 1's

over a varying number of subsequent frames depending on the truncated lower

significant bits (fig. 5 "error", 122 and dither col. 4, lines 1-14 of Pether).

It would have been obvious to one of ordinary skill in the art, at the time of the

invention, to modify Atsushi and Kitagawa to include the use of bit rate converter means

for truncating lower significant bits of the M-bit video signal, representing the truncated

lower significant bits by a different number of binary-1 's, and distributing the binary- 1's

over a varying number of subsequent frames depending on the truncated lower

significant bits as taught by Pether in order to provides a means of truncating bits since

Pether uses error feedback and dithering to reduce visual effects as stated in (col. 1,

lines 44-50 of Pether).


23.     Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Atsushi and Kitagawa, in view of Lu et. al (US 7,085,016) hereinafter, Lu.


24.     In regards to claim 7, Atsushi and Kitagawa differ from the claimed invention in

that Atsushi and Kitagawa do not explicitly disclose wherein said bit rate converter

comprises means for truncating lower significant bits of the M-bit video signal so that N

bits are left in the input video signal, and dithering the N bits according to the truncated

lower significant bits.

However, Lu teaches a system and method for wherein said bit rate converter

comprises means for truncating lower significant bits of the M-bit video signal so that N

bits are left in the input video signal, and dithering the N bits according to the truncated

lower significant bits (fig. 1 col. 2, lines 57-67 of Lu).

It would have been obvious to one of ordinary skill in the art, at the time of the

invention, to modify Atsushi and Kitagawa to include the use of dithering as taught by Lu

in order to use a process that selects approximate color from a mixture of other colors

when transition from pixel data having high bits (M bits) to pixel data having low bits (N

bits), since dithering allows for more accurately displaying graphics containing a greater

range of colors than the hardware is capable of showing as stated in (col. 1, lines 15-20

of Lu).


25.     In regards to claim 8, Atsushi and Kitagawa differ from the claimed invention in

that Atsushi and Kitagawa do not explicitly disclose an adder for a binary-1 to higher N

bits of the M-bit input video signal; a multiplexer for selecting an output of said adder or

said higher N bits of the M-bit input video signal in response to a control signal; and a

comparator for producing said control signal by making a comparison between lower

significant bits of said M-bit input video signal and a threshold value

However, Lu teaches an adder (fig. 5 (24)) for a binary-1 to higher N bits of the

M-bit input video signal; a multiplexer (fig. 5 (23)) for selecting an output of said adder or

said higher N bits of the M-bit input video signal in response to a control signal (col. 3,

lines 37-60); and a comparator (fig. 5 (22)) for producing said control signal by making a

comparison between lower significant bits of said M-bit input video signal and a

threshold value (col. 5-6, lines 37-25).

It would have been obvious to one of ordinary skill in the art, at the time of the

invention, to modify Atsushi and Kitagawa to include the use of dithering using the

particular circuit construction above as taught by Lu in order to use a process that

selects approximate color from a mixture of other colors when transition from pixel data

having high bits (M bits) to pixel data having low bits (N bits) since dithering allows for

more accurately displaying graphics containing a greater range of colors than the

hardware is capable of showing as stated in (col. 1, lines 15-20 of Lu).

### Allowable Subject Matter

26.     Claim 9 is allowed because the prior art does not contain a bit rate converter

comprising a third frame memory for storing an output of said third multiplexer; and

controller producing said first control signal only, said first and second control signals

simultaneously, or said first, second and third control signals simultaneously, depending

on truncated lower significant bits of the M-bit video signal.

27.     Claim 6 is objected to as being dependent upon a rejected base claim, but would

be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims. The prior art does not contain a bit rate converter

comprises: a third frame memory for storing an output of said third multiplexer; and

control means for producing said first control signal only, said first and second control

signals simultaneously, or said first, second and third control signals simultaneously,

depending on the truncated lower significant bits.


### *Response to Arguments*


28.     Applicant's arguments filed 9/18/2008 have been fully considered but they are

not persuasive.


29.     In response to applicant's argument that there is no suggestion to combine the

references, the examiner recognizes that obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention

where there is some teaching, suggestion, or motivation to do so found either in the

references themselves or in the knowledge generally available to one of ordinary skill in

the art.  See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re

Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).  In this case, Atsushi fails to

teach a gamma correction memory in which a plurality of N-bit input grayscale levels are

mapped to a plurality of K-bit output grayscale levels which are distributed on a non-

linear curve corresponding to a non-linear curve on which grayscale levels of a display

device are distributed.

However, Kitagawa teaches a gamma correction memory (fig. 1 (13) [0030]) in which a plurality of N-bit input grayscale levels (fig. 1 (11 bits of 13) [0020]) are mapped (fig. 7 [0029]) to a plurality of K-bit output grayscale levels which are distributed ([0020]) on a non-linear curve (fig. 7) corresponding to a non-linear curve on which grayscale levels ([0020 and 0029]) of a display device are distributed [0020].

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi to **substitute** the use of a gamma correction memory, for the memory (fig. 1 (10)) of Atsushi, as taught by Kitagawa in order to perform gamma correction in order to properly show shadow detail in RBG images and to avoid gradation deterioration in gray zones ([0005] of Kitagawa). Examiner notes that gamma correction is a non-linear relationship between pixel values and luminance. Gamma correction matters if you have any interest in displaying an image accurately on a display screen. Gamma correction controls the overall brightness of an image. Images which are not properly corrected can look either bleached out, or to dark. There is a suggestion to apply gamma correction to a signal, particularly after luminance may be alerted with a bit rate converter, to display an aesthetically pleasing image.

30.     In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning.  But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does

not include knowledge gleaned only from the applicant's disclosure, such a

reconstruction is proper.  See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA

1971).


31.     In response to applicant's argument that Atsushi does not disclose nor remotely

suggest anything about gamma correction (Remarks, page 11), the test for obviousness

is not whether the features of a secondary reference may be bodily incorporated into the

structure of the primary reference; nor is it that the claimed invention must be expressly

suggested in any one or all of the references.  Rather, the test is what the combined

teachings of the references would have suggested to those of ordinary skill in the art.

See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Examiner notes that

Atsushi is not being relied upon to teach the gamma correction but Kitagawa is being

used to teach the gamma correction. Applicant is advised to see the explanation above.


32.     The rejection of claims 3 and 4 are maintained for the reason stated above.

33.     The rejection of claim 2 is maintained for reasons stated above. In response to
Applicant contentions that Kitagawa teaches away. Teaching away requires "clear
discouragement" of the invention:

> What a reference teaches or suggests must be examined in the context of the
> knowledge, skill, and reasoning ability of a skilled artisan. What a reference
> teaches a person of ordinary skill is not, as Syntex's expert appears to believe,
> limited to what a reference specifically "talks about" or what is specifically
> "mentioned" or "written" in the reference. Under the proper legal standard, a
> reference will teach away when it suggests that the developments flowing from

its disclosures are unlikely to produce the objective of the applicant's invention. *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994). A statement that a particular combination is not a preferred embodiment does not teach away absent clear discouragement of that combination. *In re Fulton*, 391 F.3d at 1199-1200.

However, teaching away is not an issue because Kitagawa is being relied upon to teach a gamma correction unit. Lumelsky is being relied upon to teach wherein K is equal to N. (col. 5, lines 25-25)

34.    The rejection of claim 5 is maintained for the reasons stated above.

35.    The rejections of claims 7 and 8 are maintained for the reason stated above.

### *Conclusion*

36.    **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati  Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Grant D Sitta/
Examiner, Art Unit 2629
November 24, 2008